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(b) a diffusion barrier, wherein the diffusion barrier comprises a self-assembled monolayer including a plurality of molecules, each molecule having an aromatic group at the terminus of the molecule; and

(c) a metal layer on the diffusion barrier.

7. (New) The semiconductor device of claim 6 wherein the substrate comprises silicon oxide on silicon and the metal layer comprises copper.

8. (New) The semiconductor device of claim 6 wherein each molecule comprises a linear carbon chain having at least 2 carbon atoms.

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9. (New) The semiconductor device of claim 6 wherein the metal layer is a formed by a vapor deposition process.

10. (New) The semiconductor device of claim 6 wherein the diffusion barrier is capable of preventing the diffusion of metal atoms from the metal layer into the substrate when the semiconductor device is exposed to thermal annealing at 200 °C or an electric field of 2 MV/cm at 200 °C in flowing N_2.

11. (New) The semiconductor device of claim 6 wherein the diffusion barrier coats the walls of a hole in the substrate and wherein the metal layer fills the hole.

12. (New) The semiconductor device of claim 6 wherein the metal layer is in direct contact with the terminal groups of the molecules in self-assembled monolayer.

13. (New) A semiconductor device comprising:

(a) a semiconductor substrate;

(b) a diffusion barrier, wherein the diffusion barrier comprises a self-assembled monolayer including a plurality of molecules, each molecule having a linear chain at least two atoms long, and an aromatic group at the terminus of the molecule; and

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(c) a metal layer on the diffusion barrier, wherein the metal layer is formed by a vapor deposition process.

14. (New) The semiconductor device of claim 13 wherein the substrate comprises silicon oxide on silicon and the metal layer comprises copper.

15. (New) The semiconductor device of claim 13 wherein each molecule comprises a linear carbon chain having at least 2 carbon atoms.

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16. (New) The semiconductor device of claim 13 wherein the metal layer is formed by a sputtering process.

17. (New) The semiconductor device of claim 13 wherein the diffusion barrier is capable of preventing the diffusion of metal atoms from the metal layer into the substrate when the semiconductor device is exposed to thermal annealing at 200 °C or an electric field of 2 MV/cm at 200 °C in flowing N_2.

18. (New) The semiconductor device of claim 13 wherein the substrate comprises silicon oxide on silicon.

19. (New) The semiconductor device of claim 13 wherein the device does not exhibit $j_{leakage} > 1000\ nAcm^{-2}$ when the semiconductor device is exposed to thermal annealing at 200 °C or an electric field of 2 MV/cm in flowing N_2 at 200 °C for up to 650 minutes.

20. (New) The semiconductor device of claim 13 wherein the metal layer is in direct contact with the terminal groups of the molecules in self-assembled monolayer.